(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 June 2001 (14.06.2001)

PCT

(10) International Publication Number
WO 01/43176 A1

(51) International Patent Classification[7]: H01L 21/28

(21) International Application Number: PCT/KR00/01422

(22) International Filing Date: 8 December 2000 (08.12.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

1999/55862	8 December 1999 (08.12.1999)	KR
2000/3249	24 January 2000 (24.01.2000)	KR
2000/43125	26 July 2000 (26.07.2000)	KR

(71) Applicant *(for all designated States except US)*: **SAMSUNG ELECTRONICS CO., LTD.** [KR/KR]; 416, Maetan-dong, Paldal-ku, Suwon, Kyunggi-do 442-370 (KR)

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PARK, Byung-Jun** [KR/KR]; 905-1804 Jukong Apt., Youngtong-dong, Paldal-ku, Suwon, Kyunggi-do 442-470 (KR). **HWANG, Yoo-Sang** [KR/KR]; 214-806, Hankook Apt., Youngtong-dong, Paldal-ku, Suwon, Kyunggi-do 442-470 (KR).

(74) Agent: **YIM, Chang-Hyun**; Samho-Building, 3rd floor, 827-53, Yeoksam-dong, Kangnam-ku, Seoul 135-080 (KR).

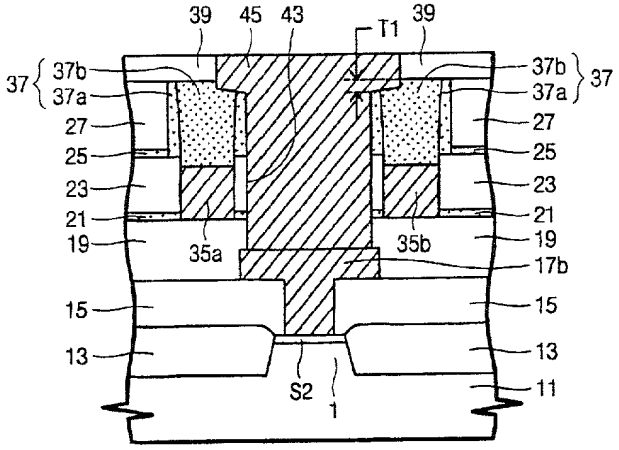
(81) Designated States *(national)*: CN, JP, US.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *With international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CONTACT STRUCTURE AND METHODS OF FORMING THE SAME



(57) Abstract: A self-aligned contact structure in a semiconductor device and methods for making such contact structure wherein the semiconductor device has a semiconductor substrate having active regions, an interlayer insulating layer covering the semiconductor substrate excluding at least a portion of each active region, at least two parallel interconnections on the interlayer insulating layer, at least one active region being relatively disposed between the at least two parallel interconnections, each interconnection having sidewalls, bottom and a width (x), a mask pattern having a top portion (z) and a bottom portion (y) formed on each interconnection, and a conductive layer pattern penetrating at least a portion of the interlayer insulating layer between the mask pattern and being electrically connected to at least one active region, wherein: $x \leq y \leq z$ and $x < z$. A second interlayer insulating layer having a relatively low dielectric constant is interposed between the conductive layer and the interconnections, which reduces the parasitic capacitance therebetween

WO 01/43176 A1